Improved Low Voltage All Cascode Mirror Current Source Using the DC Level Shifter

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Abstract- This paper presents the implementation of the so-called "DC level shifter" to obtain a low voltage, high bandwidth (200 MHz), high output resistance (11GΩ), low input resistance (0.005Ω) and low settling time (24 nSec.) cascode current mirror. The characteristics of the proposed circuit was compared with the floating gate transistor technique numerically. The simulation results in 0.5um CMOS technology indicates the superiority of the proposed method than the floating gate technology.

I. INTRODUCTION

The most common mirror topology used currently in CMOS integrated circuits is the low voltage cascode mirror [1,2]. It has moderately low input impedance, moderately low output voltage, high copying accuracy and moderately high output impedance. Since its introduction, the search is ongoing for a technology that provides both high output resistance and low output voltage. One of the interesting works is the technique presented by A. Garimella et. al. [3], which implements the floating gate transistor to lower the output voltage. The circuit characteristics would be improved significantly by this method but the floating gate transistor technique is not always applicable.

In this paper, we introduce a technique to improve the characteristics of the all cascode mirror current source, using the “DC Level Shifter”. By this method, the performance of the current source would be improved and some problems of the floating gate transistor technique are avoided.

II. THE LOW VOLTAGE IMPLEMENTATION OF ALL CASCODE MIRROR

Here is a brief description of the low voltage implementation of All Cascode Mirror (ACM) current source as described in Ref.3. Fig.1 illustrates the implemented circuit.

III. THE PROPOSED METHOD

The following figure illustrates the proposed circuit:
The DC level shifter (specified by the dashed line) was implemented instead of the floating gate transistor. In this manner, the voltage $V_x$ is equal to the difference between the overdrive voltages of transistors $M_2$ and $M_{x2}$ which work in their saturation region and draw constant currents $I_2$ and $I_i$, respectively. Assuming that $(W/L)_2=(W/L)_{x2}$, $I_2 > I_i$ and the bulk of the NMOS transistors are connected to their respective sources, $V_x$, can be written as:

$$V_x = \frac{1}{\sqrt{(W/L)_{x2} \mu_n C_{ox}/2}} \times (\sqrt{I_2} - \sqrt{I_i}) \quad (1)$$

The numerical analysis of the circuit implies that the best copying accuracy is achieved if $I_2 = 4I_i$. Substituting in Eq.1, we will get:

$$V_x = \frac{I_i}{\sqrt{(W/L)_{x2} \mu_n C_{ox}/2}} \quad (2)$$

It implies that lowering the current $I_i$ will result in $V_x$ to be decreased which lowers the output voltage of the current mirror.

The proposed circuit is most similar to the circuit presented in Ref.3 except that the NMOS cascode is implemented instead of the common source configuration and the diode-connected transistor that acts as the “DC Level Shifter” is used near the NMOS cascode amplifier. Separation of the bias currents from the input current in the proposed circuit has two advantages: 1- It reduces the input voltage requirements by one threshold voltage from $V_{GS}$ to a value that can be as low as $V_{in} = V_{DS}(sat)$ 2- It also reduces the input impedance.

IV. SIMULATION RESULTS

SPICE simulation of an implementation in a 0.5-$\mu$m CMOS technology was carried out to investigate the performance of the circuit. Bias currents with values $I_1 = 3 \mu A$ and $I_2 = 12 \mu A$, a single supply voltage $V_{dd} = 2$ V and a load resistance $R_L = 5 \Omega$ were used. Transistor dimensions (in $\mu$m) were $W/L = 50/1.2$ for $M_1$, $M_{IC}$, $M_2$, $M_{x2}$ and $W/L = 5/1.2$ for other transistors. Fig.3-a shows the DC output characteristics of the proposed circuit with $I_m$ parameterized from 20 $\mu A$ to 100 $\mu A$ in 20 $\mu A$ steps and Fig.3-b illustrates the minimum output voltage versus the current $I_1$.

As we described earlier, Fig.3-b implies that by decreasing the current $I_1$, the minimum output voltage would be decreased.

Compared to the floating gate transistor technique, the output resistance was increased from 8$\Omega$ to 11$\Omega$, the output voltage was decreased from 0.15V to 0.11V and the copying accuracy was improved from around 0.1% to 0.05%.

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REFERENCES

